APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/520,677	03/07/2000	Garry Z. Gu	56115534-120430	9129

26291 7590 05/04/2004		EXAMINER	
MOSER, PATTERSON & SHERIDAN L.L.P.		VOLPER, THOMAS E	
595 SHREWSBURY AVE, STE 100			
FIRST FLOOR		ART UNIT	PAPER NUMBER
SHREWSBURY, NJ 07702		2665	

DATE MAILED: 05/04/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-12 and 15-17* is/are rejected.

7)☒ Claim(s) *6-9, 13, 14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 24 February 2004 have been fully considered but they are not persuasive.

2.   Applicant argues that the language in the Larsson reference, such as "one could conceive a solution without a separate control unit…" and "(input ports would) easily calculate how many cells can be permitted to be sent…", indicates that Larsson is essentially not interested in the specifics that performs the calculations (page 3, 2nd paragraph of "Remarks"). However, the Examiner notes that, "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." *In re Heck*, 699 F.2d 1331, 1332-33, 216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting *In re Lemelson*, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). Furthermore, Applicant argues that the criteria for combining references in an obviousness rejection is not what the prior art "represents", to quote the Examiner from the previous Office action, but what the prior art *teaches*. To clarify the position of the Examiner from the previous Office action, it is noted that the term "represents" was used to indicate that a portion of the prior art met the limitations of a particular portion of the present invention. In view of the case law cited above and the clarification of the Examiner's position, it is clear that the Larsson reference *teaches* the function of an integrator block in each input port. Since Larsson shows multiple input ports together in a group, Larsson also *teaches* neighboring

integrator blocks. Also, as can be seen in Figure 3, Larsson shows input ports (2-4) and output

ports (5-7) in equal numbers, thus meeting the limitation of corresponding integrator blocks.

Applicant also argues that Larsson does not provide any specific description of how the

calculations are performed and is "too general to derive a specific teaching of elements in Claim

1" (page 4, 1st paragraph of "Remarks"). However, Claim 1 of the present invention gives no

specific description of how any calculations are performed. The closest the claim comes to a

description of any calculation is "an integrator block for receiving a token bit and updating a

grant credit," which clearly is not a specific description of how a calculation is performed, but

rather just a statement that some calculation is performed. A grant credit is updated, but there is

no description of how it is updated. Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van*

Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Larsson teaches, as described above,

that the input ports could, with information based on the fullness of the output buffers, be able to

"easily calculate how many cells can be permitted to be sent in the next time interval" (col. 5,

lines 16-24). This meets the limitation of an integrator block in each input port, and is at least as

specific as Claim 1, except for the way the fullness of the output buffers is conveyed to the input

ports, i.e. receiving a token bit, which is provided by Caldara.

Applicant asserts that the Examiner has used impermissible hindsight when stating, "It is

obvious that some component, such as a statistic block as in the present application, must count

the number of cells in the output buffers and compare them..." (page 4, 2nd paragraph of

"Remarks"). In response to Applicant's assertion that the Examiner's conclusion of obviousness

is based upon improper hindsight reasoning, it must be recognized that any judgment on

obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The functionality of determining whether output buffers have reached a threshold level is present in the Caldara reference (col. 4, lines 37-53), and is not borrowed from Applicant's disclosure. The fullness of the output buffers is reflected in a feedback message that contains an ACCEPT/REJECT bit (col. 5, line 64 – col. 6, line 14). The Examiner maintains that this ACCEPT/REJECT bit meets the limitation of a token bit as described in the present invention. The statement made by the Examiner in the previous Office action purports to establish that since the functionality of sending a token bit based on some determination is present in the reference, it is obvious that some physical device, meeting the limitation of the statistic block in the present invention, must be present to perform that action. That statement, as the Applicant suggests, does not attempt to use a part of the Applicant's disclosure to reconstruct the present invention, but rather states what feature of the present invention is being met by a particular description in the Caldara reference.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1-5, 10-12 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Larsson et al. (US 6,172,963) in view of Caldara et al. (US 5,978,359).

Regarding claim 1, 10, 11 and 15, Larsson discloses a credit-based flow control system

for a switch with input and output buffers. The input and output buffers meet the limitation of

first and second stage port processors as in the present invention. The system takes into account

the degree of fullness of the output buffers when determining how many cells (credits) can be

sent from each input port. This process is called "giving credit" (col. 3, lines 21-30). With

intelligence in the switch, it can be determined which output ports are able to receive cells (col.

4, lines 45-55). In the preferred embodiment, Larsson discloses a control unit (20) located in the

switch core (8) for performing the intelligence. However, the intelligence may also be located

outside the switch core and incorporated into the input buffers. In this case, the input ports

would read the degree of fullness of the output buffers and calculate how many cells can be sent

(col. 5, lines 12-23). This description meets the limitation of an integrator block in a first stage

port processor, as in the present application. The limitation of neighboring integrator blocks is

met by Larsson in that calculating the number of cells to be sent to a particular output buffer

includes determining which input ports should be allowed to send cells if several input ports are

competing for the output buffer (col. 5, lines 31-36). Larsson shows input ports (2-4) and output

ports (5-7) in equal numbers, thus meeting the limitation of corresponding integrator blocks

(Figure 3). Larsson fails to expressly disclose sending a token bit from a second stage port

processor to the neighboring first stage port processors. Caldara discloses a switching

architecture that includes a first set of port processors, called To Switch Port Processors (TSPP)

(14) and a second set of port processors, called From Switch Port Processors (FSPP) (16). These

sets of TSPP's and FSPP's can be construed as first and second stages in the switch, respectively.

Caldara also discloses a feedback message (30) that provides an indication of buffer status at the

output port. To provide efficient flow control, the feedback message from the output port to the

input port includes several sub-type messages, including an ACCEPT/ REJECT bit (col. 5, line

64 – col. 6, line 14). This bit is considered to provide the function of the token bit of the

applicant's invention. Caldara discloses it is determined if the output buffers become filled to a

threshold level when sending the feedback message in order to prevent cell loss (col. 4, lines 37-

53). It is obvious that some component must be present to count the number of cells in the

output buffers and compare them to a threshold level in order to provide the functionality

disclosed in the cited passage. This component would meet the limitation of a statistic block as

described in the present application. At the time the invention was made, it would have been

obvious to a person of ordinary skill in the art to use the feedback message of Caldara in

combination with the credit based flow control system of Larsson to provide a switch that

selectively sends data from a first stage of input ports to a second stage of output ports in

accordance with the fullness or availability of each output buffer. The feedback message of

Caldara would notify the intelligent input ports of Larsson as to the availability of the output

ports in order to calculate the credit given to each input port. One of ordinary skill in the art

would have been motivated to do this to provide efficient flow control and avoid cell loss in the

switch.

Regarding claims 2 and 3, Larsson discloses multiple input ports. The aforementioned

teaching regarding claims 1, 10, 11 and 15 provides a description for the incorporation of

intelligence into the input port. This description provides for an equivalent to neighboring

integrator blocks.

Regarding claims 4, 5, 12, 16 and 17, Larsson discloses that the number of cells (credits)

that can be sent are calculated for a time interval and depend on the number of cells already in

the output buffers (col. 3, lines 45-58). Depending on the fullness of the output buffers from

interval to interval, that the number of credits will change. This effectively achieves the process

of incrementing and decrementing credits between time intervals.

Allowable Subject Matter

5.   Claims 6-9, 13, 14 and 18 are objected to as being dependent upon a rejected base claim,

but would be allowable if rewritten in independent form including all of the limitations of the

base claim and any intervening claims.

Conclusion

6.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

7.   Any inquiry concerning this communication, or earlier communications from the

examiner should be directed to Thomas Volper whose telephone number is 703-305-8405 and

fax number is 703-746-9467. The examiner can normally be reached between 8:30am and

6:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Huy Vu, can be reached at 703-308-6602. Any inquiry of a general nature or relating

to the status of this application or proceeding should be directed to the receptionist whose

telephone number is 703-305-4750.

Thomas E. Volper

April 29, 2004

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600